SUBSTITUTE SPECIFICATION

A Low Phase Noise MOS LC Oscillator

[0001] This application is a continuation of, and hereby claims priority under 35 U.S.C. §120 on, U.S. application serial number 09/669,772 filed on October 30, 2000, the entire contents of which are hereby incorporated herein by reference, which is based on, and which claims priority under 35 U.S.C. §120 on, provisional patent application, 60/204,885, filed on May 17, 2000.

Background of the Invention

Field of the Invention

[0002] This invention relates to high frequency oscillator circuits. More particularly, this invention relates to metal oxide semiconductor (MOS) oscillators having low phase noise.

Description of the Related Art

[0003] Inductive/capacitive (LC) oscillators are important elements of any Radio Frequency (RF) communication devices, such as transmitters, where the LC oscillators are used as master oscillators, or as receivers where the LC

oscillators are used as local oscillators. An important performance benchmark of an LC oscillator is the phase noise characteristic. An oscillator with a lower phase noise indicates that the oscillator produces lower spurious energy outside the desired fundamental signal tone.

[0004] Phase noise is produced as a result of low frequency noise signal found in active elements used in the oscillator. This low frequency signal is modulated (up converted) by the fundamental signal tone, resulting in the spreading of the oscillator frequency energy beyond the intended target frequency. This low frequency noise signal source is often referred to as flicker noise (commonly referred to in the literature as 1/f) in bipolar and Metal Oxide Semiconductor (MOS) transistors. The 1/f noise energy in bipolar transistors is known to be significantly less than that of MOS transistors. This is the reason why practically all low phase noise LC oscillators are built using bipolar transistors or even more esoteric transistors such as Galium-Arsenide devices.

[0005] Complementary MOS (CMOS) based LC oscillators are now being investigated again for application to systems-on-a-chip (SOC) devices for RF communication applications. LC oscillators of the prior art fall far short of the minimum performance requirements of many of today's wireless communication systems.

[0006] A typical example of an LC oscillator in MOS technology is shown in

Fig. 2. It is based on cross-coupled NMOS transistors **M1** and **M2**, a pair of inductors **L1** and **L2**, and capacitor **C1** and **C2** tuning elements. PMOS transistors, which usually have slightly lower 1/f noise characteristics, can be used to replace the NMOS transistors **M1** and **M2** at a slight increase in power dissipation and lower maximum operating frequency.

[0007] A review of a general form of the criteria for designing an oscillator circuit of the prior art is shown in Fig. 1. The necessary components of an oscillator are a frequency dependent gain circuit **100**, a frequency dependent feedback circuit **105**, and a combining block **110**. The output V_0 **120** of the gain circuit **100** is the input to the feedback circuit **105**. The input signal V_1 **115** is combined in the combining block **110** with the output V_{fb} **107** of the feedback circuit **105** to form the input **112** of the gain circuit **100**.

[0008] The gain of the gain block **100** is designated **G(jω)** and the gain of the feedback circuit **105** is designated **H(jω)**. These gains **G(jω)** and **H(jω)** describe the relationship of their respective output signals V_o **120** and V_{fb} **107** to their respective input signals **112** and V_o **120**. Therefore, the output signal V_o **120** becomes

$$V_o = \frac{V_i G(j\omega)}{1 + G(j\omega)H(j\omega)}.$$

[0009] For an oscillator, the output signal V_o **120** must be nonzero even if the input voltage V_1 **115** is zero. For this to be true, then

$$1 + G(j\omega)H(j\omega) = 0$$

or

$$G(j\omega)H(j\omega) = -1.$$

That is, the magnitude of the open-loop transfer function must be equal to 1 and the phase shift of the gain circuit **100** and the feedback circuit **105** must be 180°.

[0010] In Fig. 2, the gain circuit of the oscillator is formed by the differentially cross-connected pair of transistors **M1** and **M2** and the constant current source **I1**. The frequency dependent gain determining impedances are formed by the inductors **L1** and **L2** and the capacitors **C1** and **C2**.

[0011] The feedback circuit is accomplished by the connecting of the drain of the NMOS transistor **M1** to the gate of the NMOS transistor **M2** and the drain of the NMOS transistor **M2** to the gate of the NMOS transistor **M1**. This forms a cross-coupled differential oscillator.

[0012] A CMOS oscillator of the prior art is illustrated in Fig. 3. In this case, the gain circuit is formed by the differentially connected pair of NMOS transistors **M1** and **M2**, the differentially connected pair of PMOS transistors **M3** and **M4**, and the current sources **I1** and **I2**. As described above, the frequency dependent gain determining impedances are formed by the inductors **L1** and **L2**

and capacitors **C1** and **C2**.

[0013] The fundamental frequency f0 of a cross coupled differential oscillator is determined by the formula:

$$\omega = \frac{1}{\sqrt{L_{eff}C_{eff}}} \text{ such that}$$

$$f_o = \frac{1}{2\pi\sqrt{L_{eff}C_{eff}}}$$

where:

L_{eff} is the value of the effective inductance of the inductors **L1** and **L2**.

C_{eff} is the value of the effective capacitance of the capacitors **C1** and **C2**.

For the structure of the design where the inductors are mutually coupled then the effective inductance is:

$$L_{eff} = 4L1 = 4L2 .$$

The effective capacitance of the capacitors **C1** and **C2** is the parallel combination of the two capacitors **C1** and **C2** and is:

$$C_{eff} = \frac{1}{2}C1 = \frac{1}{2}C2$$

Combining the above, the frequency of the oscillators of Figs. 2 and 3 is:

$$f_o = \frac{1}{2\pi\sqrt{2L1C2}}.$$

It should be noted that the capacitances **C1** and **C2** included the parasitic capacitances of the oscillator circuit.

[0014] It is well known in the art that phase noise is the result of small perturbations in phase due to small random shifts in oscillator frequency. These shifts are caused by thermal noise, shot noise, and flicker noise (1/f noise). These noises are functions of the device characteristics of the NMOS transistors **M1** and **M2** of Figs. 2 and 3 and the PMOS transistors **M3** and **M4** of Fig. 3. The phase noise is modeled as small voltage sources **Vn1** and **Vn2** at the gates of the NMOS transistors **M1** and **M2** of Figs. 2 and 3 and voltage sources **Vp1** and **Vp2** at the gates of the PMOS transistors **M4** and **M4** of Fig. 3.

[0015] This flicker noise (1/f noise) is a function of the active device characteristics of the NMOS transistors **M1** and **M2** of Figs. 1 and 2 and PMOS transistors **M3** and **M4** of Fig. 3.

[0016] The advancements in scaling of the device features in semiconductor processing allow multi-gigahertz operating frequencies to be readily achievable. Unfortunately, the same scaling down of MOS transistors have the opposite effect on the 1/f noise characteristics. The smaller device geometries are, the higher the 1/f noise components, leading to higher phase noise on the final

oscillator.

[0017] "A 1.8 Ghz CMOS Voltage-Controlled Oscillator", - Razavi, B., Digest of Technical Papers. 43rd ISSCC, 1997, pp. 388 - 389 and shown in Fig. 4 describes a structure of having multiple oscillators **OSC1** and **OSC2** coupled together to oscillate in quadrature or 90° out-of-phase. The oscillators **OSC1** and **OSC2** are structured and function as described in Fig. 2. The differential pair of NMOS transistors **M3** and **M4** and the current source **I2** form a first coupling circuit. The first coupling circuit has an in-phase input that is formed by the gate of the NMOS transistors **M3** and a out-of-phase input that is formed by the gate of the NMOS transistor **M4**. The first coupling circuit has a in-phase output that is formed by the drain of the NMOS transistor **M4** and an out-of-phase output that is formed by the drain of the NMOS transistor **M3**. The in-phase input of the first coupling circuit is connected to the drain of the NMOS transistor **M5** and the gate of the NMOS transistor **M6**. The out-of-phase input of the first coupling circuit is connected to the drain of the NMOS transistor **M6** and the gate of the NMOS transistor **M5**. The in-phase output of the first coupling circuit is connected to the drain of the NMOS transistor **M2** and the gate of the NMOS transistor **M1**. The out-of-phase output of the first coupling circuit is connected to the drain of the NMOS transistor **M1** and the gate of the NMOS transistor **M2**.

[0018] The differential pair of NMOS transistors **M7** and **M8** and the current

source **I4** form a second coupling circuit. The second coupling circuit has an in-phase input that is formed by the gate of the NMOS transistors **M7** and a out-of-phase input that is formed by the gate of the NMOS transistor **M8**. The second coupling circuit has a in-phase output that is formed by the drain of the NMOS transistor **M8** and an out-of-phase output that is formed by the drain of the NMOS transistor **M7**. The in-phase input of the second coupling circuit is connected to the drain of the NMOS transistor **M2** and the gate of the NMOS transistor **M1**. The out-of-phase input of the second coupling circuit is connected to the drain of the NMOS transistor **M1** and the gate of the NMOS transistor **M2**. The in-phase output of the second coupling circuit is connected to the drain of the NMOS transistor **M6** and the gate of the NMOS transistor **M5**. The out-of-phase output of the second coupling circuit is connected to the drain of the NMOS transistor **M6** and the gate of the NMOS transistor **M5**.

[0019] The structure as shown generates two oscillatory signals, one between the drains of the NMOS transistors **M1** and **M2** and one between the drains of the NMOS transistors **M5** and **M6**. The two oscillatory signals are in quadrature or 90° out of phase. The quadrature oscillator as described is subject to the phase noise problems as above-described.

[0020] "Design Issues In CMOS Differential LC Oscillators," Hajimiri, A., Lee, T.H., IEEE Journal of Solid-State Circuits, pp. 717 - 724, May 1999 Vol. 34 Issue No. 5, presents an analysis of phase noise in differential cross-coupled

inductance-capacitance (LC) oscillators. The effect of tail current and tank power dissipation on the voltage amplitude is shown. Various noise sources in the complementary cross-coupled pair are identified, and their effect on phase noise is analyzed.

[0021] "Phase Noise In CMOS Differential LC Oscillators", Hajimiri, A., Lee, T.H., Digest of Technical Papers -1998 Symposium on VLSI Circuits, 1998, pp. 48 - 51, describes an analysis of phase noise in differential cross-coupled tuned tank voltage controlled oscillators. The effect of active device noise sources as well as the noise due to the passive elements is taken into account.

[0022] U. S. Patent 5,475,345 (Gabara) teaches a CMOS coupled-tank oscillator having two inverters coupled, input-to-output, by inductances that may be simply wires, and a capacitance acting in parallel with each inverter that may be, simply, the inverter's gate capacitance.

[0023] U. S. Patent 5,850,163 (Drost, et al.) discusses an active inductor oscillator with wide frequency range. The active inductor oscillator includes a tank circuit, buffer and integrating circuit that use differential transistor pairs that reduce phase jitter due to external common-mode noise sources.

[0024] U. S. Patent 5,959,504 (Wang) describes a voltage controlled oscillator CMOS circuit using back gate terminals of CMOS transistors to vary the parasitic

capacitances of the transistors. The back gate terminals receive a signal from a variable voltage source so that oscillation can be controlled by adjusting the variable voltage.

[0025] "A Low-Noise, 900-MHz VCO in 0.6-um CMOS" (Park, et al), IEEE Journal Of Solid-State Circuits, Vol. 34, pp. 586 - 591, May 1999, Issue No. 5, describes a low-noise, 900-MHz, voltage controlled oscillator (VCO) fabricated in a 0.6-um CMOS technology. The VCO consists of four-stage fully differential delay cells performing full switching. It utilizes dual-delay path techniques to achieve high oscillation frequency and obtain a wide tuning range.

[0026] "10MHz CMOS OTA-C Voltage-Controlled Quadrature Oscillator," Linares-Barranco, et al., IEEE Electronics Letters, June 1989, pp. 765-767, Vol. 25, Issue No. 12, details a quadrature-type voltage-controlled oscillator with operational transconductance amplifiers and capacitors (OTA-C).

[0027] "RC Sequence Asymmetric Polyphase Networks for RF Integrated Transceivers," Galal et al, Transactions On Circuits And Systems - II: Analog And Digital Signal Processing, January 2000, pp. VOL 47, Issue No. 1, describes Resistance-Capacitance (RC) sequence asymmetric polyphase networks. A sequence of asymmetric polyphase networks provide the generation of highly matched wide-band quadrature signals which are immune to components mismatch, and suppression of the image signals without the need for highly

selective RF filters and without employing image-reject mixing techniques.

[0028] U. S. Patent 5,714,911 (Gilbert) describes a quadrature oscillator that includes an amplitude control circuit. The amplitude control circuit is that is based upon the trigonometric identity $\sin^2(\Omega t)+ \cos^2(\Omega t)=1$. The amplitude control circuit, referred to as a Pythagorator, includes two squaring circuits. Each squaring circuit receives a respective quadrature oscillator signal and squares it. The outputs of the two squaring circuits are joined together so as to sum the outputs of the two squaring circuits to produce a sum of squares signal. This signal, a current in the preferred embodiment, is provided to damping diodes coupled to the outputs of the quadrature oscillator. The damping diodes produce a shunt positive resistance at the outputs of the quadrature oscillator in response to this current that has the effect of canceling the shunt negative resistance of the regenerative elements of the oscillator thereby establishing the amplitude of the quadrature oscillator signals at a desired amplitude.

[0029] U. S. Patent 5,949,295 (Schmidt) teaches an integratable tunable resonant circuit for use in filters and oscillators. The circuit incorporates differential amplifier stage with a pair of differentially connected transistors with two negative feedback resistors. The two negative feedback resistors increase the linearity range of an input voltage of the differential amplifier stage.

[0030] U. S. Patent 6,008,701 (Gilbert) details a quadrature oscillator using

inherent nonlinearities of impedance cells to limit amplitude. The quadrature oscillator based on two cross-coupled integrator cells utilizing the inherent nonlinearity of positive and negative impedance cells to control the amplitude of oscillation. The oscillator is simplified thus eliminating the need for an outer control loop. A negative impedance cell is coupled to each integrator cell for assuring proper start-up and enhancing the amplitude of oscillation. A positive impedance cell is also coupled to each integrator cell to dampen the amplitude of oscillation. The transconductance of each impedance cell varies in response to the bias current provided to the cell. Thus, by controlling the bias currents through the cells, the negative and positive impedances seen by each integrator cell can made to cancel at the desired oscillation amplitude, so that the circuit oscillates without any damping or enhancement. By utilizing the inherent nonlinearity of positive and negative impedance cells, the bias currents provided to the impedance cells can remain fixed for a given frequency of operation, thereby simplifying the design of the oscillator and providing precise, robust control.

Summary of the Invention

[0031] An object of this invention is to provide a cross-coupled differential MOS oscillator.

[0032] Another object of this invention is to provide a cross-coupled differential MOS oscillator having reduced phase noise.

[0033] Another object of this invention is to provide a RF communication device, e.g., a transmitter or receiver, having a cross-coupled differential MOS oscillator.

[0034] To accomplish these and other objects, an oscillator having low phase noise that is formed of a frequency dependent amplifier to amplify a signal having a fundamental frequency; a frequency dependent feedback device that is connected between an output of the frequency dependent amplifier and an input of the frequency dependent amplifier to feed a portion of an amplified signal having the fundamental frequency to an input of the frequency dependent amplifier to stimulate oscillation; and a attenuating device in communication with the frequency dependent amplifier. The attenuating device reduces the gain of the frequency dependent amplifier for signals having frequencies much, much less than the fundamental frequency to decrease the phase noise.

[0035] The frequency dependent amplifier has an amplifying means. The amplifying means has an input and an output, whereby a signal at the input is amplified by a gain factor to form a signal at the output. The frequency dependent amplifier further, has a frequency dependent gain determining in communication with the amplifying means. The frequency dependent gain determining impedance determines the frequency at which the maximum gain of the frequency dependent amplifier occurs.

[0036] The amplifying means is composed of a pair of cross-coupled MOS transistors. The drain of each MOS transistor is connected to a gate of the other MOS transistor and to a port of the frequency dependent gain determining impedance. A first current source is connected to a source of one of the MOS transistors and to a ground reference point and to a first port of the attenuating device. A second current source is connected to a source of the other MOS transistor and to a second port of the attenuating device.

[0037] The frequency dependent determining impedance is formed by at least one inductor in communication with the amplifying means and a power supply voltage source, and at least one capacitor in communication with the amplifying means and a ground reference point.

[0038] The attenuating device is in the preferred embodiment, a capacitor in communication with the sources of the cross-coupled MOS transistors. The value of the capacitor is selected such that the fundamental frequency of oscillation is from approximately 10 times to approximately 20 times the high pass bandwidth of the cross-coupled MOS transistors.

[0039] Alternately, the amplifying means is formed of a cross-coupled pair of MOS transistors of the first conductivity type and a cross-coupled pair of MOS transistors of the second conductivity type to form a CMOS amplifying means. The drain of each MOS transistor of the first conductivity type is connected to a

gate of the other MOS transistor of the first conductivity type and to a port of the frequency dependent gain determining impedance. A first current source is connected to a source of one of the MOS transistors of the first conductivity type and to a first port of the attenuating device, and a second current source is connected to a source of the other MOS transistor of the first conductivity type and to a second port of the attenuating device.

[0040] The drain of each MOS transistor of the second conductivity type is connected to a gate of the other MOS transistor of the second conductivity type and to one port of the frequency dependent gain determining impedance. A third current source in communication with a source of one of the MOS transistors of the second conductivity type and to a third port of the attenuating device, and a fourth current source in communication with a source of the other MOS transistor of the second conductivity type and to a fourth port of the attenuating device.

[0041] The attenuating device in the CMOS embodiment of the amplifying means is composed of a first capacitor connected from the first port to the second port of the gain attenuating means and a second capacitor in communication with the third and fourth ports of the gain attenuating means.

[0042] An application of the cross-coupled differential MOS oscillator is as the carrier oscillator of an RF transmitter. Alternately, the cross-coupled differential MOS oscillator is the local oscillator of an RF receiver that is used to demodulate

the incoming RF signal.

Brief Description of the Drawings

[0043] Fig. 1 is a system block diagram of a frequency dependent system with feedback of the prior art.

[0044] Fig. 2 is a schematic diagram of a cross-coupled differential NMOS oscillator of the prior art.

[0045] Fig. 3 is a schematic diagram of a cross-coupled differential CMOS oscillator of the prior art.

[0046] Fig. 4 is a schematic diagram of a quadrature oscillator of the prior art.

[0047] Figs. 5a and 5b are schematic diagrams of two embodiments of cross-coupled differential MOS oscillators of this invention.

[0048] Fig. 6a and 6b are schematic diagrams of the cross-coupled differential MOS oscillator of this invention (Fig. 5a) operating at low frequencies (Fig. 6a) and at high frequencies (Fig. 6b).

[0049] Fig. 7 is a schematic diagram of a cross-coupled differential CMOS oscillator of this invention.

[0050] Fig. 8 is a schematic diagram of a quadrature oscillator having low phase noise of this invention having.

[0051] Fig. 9 is a block diagram of a multiple frequency transforming circuit having low phase noise of this invention.

[0052] Fig. 10 is a schematic diagram of a differential amplifier having low phase noise of this invention.

[0053] Fig. 11 is a plot of the spectral density of the phase noise versus the frequency offset from the fundamental frequency.

[0054] Fig. 12a is a schematic diagram of an ideal current source implemented by a biased MOSFET.

[0055] Fig. 12b is a schematic diagram of a current source of Fig. 12a having the noise component represented as a voltage source.

[0056] Fig. 12c is a schematic diagram of a current source of Fig. 12a having the noise component represented as a parallel current source.

[0057] Fig. 13a is a current source implemented as a programmable

resistance.

[0058] Fig. 13b is an example of a programmable resistance of Fig. 13a.

[0059] Fig. 14a is a current source implemented as an inductance and programmable resistance.

[0060] Fig. 14b is an example of a programmable resistance of Fig. 14a.

[0061] Fig. 14c is an example of a programmable inductance/resistance of Fig. 14a.

Detailed Description of the Invention

[0062] Refer now to Fig. 5a for a discussion of the cross-coupled differential NMOS oscillator having low phase noise of this invention. The frequency dependent gain amplifier is formed by the NMOS transistors **M1** and **M2** and the constant current sources **I1** and **I2**. The frequency dependent gain determining impedance is formed by the inductors **L1** and **L2** and the capacitors **C1** and **C2**.

[0063] The inductor **L1** is connected from the drain of the NMOS transistor **M1** to the reference voltage source V_{CC} and the inductor **L2** is connected from the drain of the NMOS transistor **M2** to the reference voltage source V_{CC}. The capacitor **C1** is connected from the drain of NMOS transistor **M1** to the ground reference point and the capacitor **C2** is connected from the drain of the NMOS

transistor **M2** to the ground reference point. It is apparent to those skilled in the art that, while the capacitors **C1** and **C2** are connected to the ground reference point, the capacitors **C1** and **C2** may be connected to any reference voltage source or to any power supply voltage source and not effect the operation of the oscillator as explained above.

[0064] The fundamental frequency f_0 of the cross-coupled differential oscillator of this invention is determined as:

$$\omega = \frac{1}{\sqrt{2L_1C_1}} \quad \text{such that}$$

$$f_0 = \frac{1}{2\pi\sqrt{2L_1C_1}}$$

where:

L_1 is the value of the inductance of the inductor **L1** or **L2**.

C_1 is the value of the capacitance of the capacitor **C1** or **C2**.

[0065] The drain of the NMOS transistor **M1** is connected to the gate of the NMOS transistor **M2** and the drain of the NMOS transistor **M2** is connected to the gate of the NMOS transistor **M1**. This cross-coupling of the drains to the gates of the NMOS transistors **M1** and **M2** forms the feedback circuit of the oscillator.

[0066] The source of the NMOS transistor **M1** is connected to the constant current source **I1** and the source of the NMOS transistor **M2** is connected to the constant current source **I2**. The decoupling capacitor C_C is connected between the sources of the NMOS transistors **M1** and **M2** to act as a gain-attenuating device.

[0067] Refer now to Figs. 6a and 6b to understand the operation of the cross-coupled differential oscillator of this invention. The decoupling capacitor C_C is chosen to have very high impedance at frequencies much, much lower than the fundamental frequency f_0 of the cross-coupled differential NMOS oscillator of Fig. 6a. At frequencies much lower than the fundamental frequency f_0, the cross-coupled differential NMOS oscillator of this invention functions as shown in Fig. 6a. The current sources are separated and the gain of the frequency dependent gain circuit formed by the NMOS transistors **M1** and **M2** and the current sources **I1** and **I2** becomes much, much less than one, preventing the flicker noise or 1/f noise of the noise voltage sources **Vn1** and **Vn2** from being amplified and being added to the output signal of the cross-coupled differential NMOS oscillator of this invention.

[0068] At the fundamental frequency f_0, the decoupling capacitor C_C is chosen to have an impedance that is very low. Thus, the cross-coupled differential NMOS oscillator of this invention functions as shown in Fig. 6b. The frequency

dependent gain circuit formed by the NMOS transistors **M1** and **M2** and the constant current sources **I1** and **I2** function as described in Fig. 2. The constant current sources **I1** and **I2** are summed together to form effectively one current source (**I1+I2**). Thus, the frequencies at the fundamental frequency f_0 are amplified. The frequency dependent gain determining impedance formed by the inductors **L1** and **L2** and the capacitors **C1** and **C2** insure that the peak gain of the frequency dependent gain circuit is at the fundamental frequency f_0 and that the higher and lower frequencies are attenuated.

[0069] The noise voltage sources **Vn1** and **Vn2** are, as described above, the models of the flicker or 1/f noise that is caused by the device characteristics of the NMOS transistors **M1** and **M2**. The noise voltage sources **Vn1** and **Vn2** having frequency content that is much less than the fundamental frequency f_0 and thus will be attenuated as shown in Fig. 6a.

[0070] The high pass bandwidth (**BW**) of the cross-coupled differential oscillator is a function of the transconductance of the NMOS **M1** and **M2** and the value of the decoupling capacitor **Cc** and is determined by the formula:

$$BW = \frac{g_m}{2\pi Cc}.$$

[0071] The high pass bandwidth **BW** must be maintained at a level that is much, much smaller than the cutoff frequency of the cross-coupled differential oscillator to prevent loss of the fundamental frequency signal. The decoupling

capacitor **Cc** should be chosen such that the fundamental frequency f0 of the cross-coupled differential oscillator is from approximately ten times to approximately twenty times the high pass bandwidth **BW** of the cross-coupled oscillator.

[0072] Fig. 5b illustrates a second embodiment of a cross-coupled differential NMOS oscillator of this invention. The frequency dependent gain amplifier in this case is formed by the NMOS transistors **M1** and **M2** and the resistors **R1** and **R2**. The resistor **R1** is connected between the source of the NMOS transistor **M1** and the ground reference point. The resistor **R2** is connected between the source of the NMOS transistor **M2** and the ground reference point.

[0073] The inductor **L1** is connected from the drain of the N MOS transistor **M1** to the reference voltage source V_{cc} and the inductor **L2** is connected from the drain of the NMOS transistor **M2** to the reference voltage source V_{cc}. The capacitor **C1** is connected from the drain of NMOS transistor **M1** to the ground reference point and the capacitor **C2** is connected from the drain of the NMOS transistor **M2** to the ground reference point. As described above, it is apparent to those skilled in the art that, while the capacitors **C1** and **C2** are connected to the ground reference point, the capacitors **C1** and **C2** may be connected to any reference voltage source or to any power supply voltage source and not effect the operation of the oscillator.

[0074] The decoupling capacitor **Cc2** is connected between the sources of the NMOS transistors **M1** and **M2** and acts as gain attenuating device as above-described.

[0075] A third embodiment of this invention, as shown in Fig. 7, implements the frequency dependent gain circuit as a cross-coupled differential CMOS amplifier. The frequency dependent gain circuit is formed by the NMOS transistors **M1** and **M2**, the P-type MOS (PMOS) transistors **M3** and **M4**, and the current sources **I1**, **I2**, **I3**, and **I4**.

[0076] The drain of the NMOS transistor **M1** is connected to the gate of the NMOS transistor **M2** and the drain of the NMOS transistor **M2** is connected to the gate of the NMOS transistor **M1**. Similarly, the drain of the PMOS transistor **M3** is connected to the gate of the PMOS transistor **M4** and the drain of the PMOS transistor **M4** is connected to the gate of the PMOS transistor **M3**. The cross-coupling of the drains and gates of the NMOS transistors **M1** and **M2** and the PMOS transistors **M3** and **M4** forms the feedback circuit of the oscillator.

[0077] The inductor **L1** is connected between the drains of the NMOS and PMOS transistors **M1** and **M3** and the reference voltage source V_{CT}. The inductor **L2** is connected between the drains of the NMOS and PMOS transistors **M2** and **M4** and the reference voltage source V_{CT}. The capacitor **C1** is connected between the drains of the NMOS and PMOS transistors **M1** and **M3**

and the ground reference point. The capacitor **C2** is connected between the drains of the NMOS and PMOS transistors **M2** and **M4** and the ground reference point. Again, as described above, it is apparent to those skilled in the art that, while the capacitors **C1** and **C2** are connected to the ground reference point, the capacitors **C1** and **C2** may be connected to any reference voltage source or to any power supply voltage source and not effect the operation of the oscillator.

[0078] The inductors **L1** and **L2** and the capacitors **C2** and **C2** form the frequency dependent gain determining impedance.

[0079] The constant current source **I1** is connected to the source of the NMOS transistor **M1**, and the constant current source **I2** is connected to the source of the NMOS transistor **M2**. Similarly, the constant current source **I3** is connected to the source of the PMOS transistor **M3** and the constant current source **I4** is connected to the source of the PMOS transistor **M4**.

[0080] The gain-attenuating circuit is formed by the decoupling capacitors C_C3 and C_C4. The decoupling capacitor C_C3 is connected between the sources of the NMOS transistors **M1** and **M2**. The decoupling capacitor C_C4 is connected between the sources of the PMOS transistors **M3** and **M4**.

[0081] The gain-attenuating circuit (C_C3 and C_C4) functions much as described in Figs. 6a and 6b. For frequencies much, much less than the

fundamental frequency f_0, the decoupling capacitors C_C3 and C_C4 have a large impedance and force the gain of the frequency dependent gain circuit to a level much, much less than one to attenuate the low frequency flicker or 1/f noise. Conversely, for frequencies equal to the fundamental frequency f_o, the decoupling capacitors **Cc3** and **Cc4** have low impedance and the frequency dependent gain circuit functions equivalently to that as described in Fig. 3. The constant current sources **I1** and **I2** are summed as described in Fig. 5b and, similarly, the constant current sources **I3** and **I4** are summed together to function equivalently to the description of Fig. 3.

[0082] The high pass bandwidth (**BW**) of the cross-coupled differential oscillator is a function of the transconductance of the NMOS **M1** and **M2** and the value of the decoupling capacitor **Cc3** and the transconductance of the PMOS transistors **M3** and **M4** and the value of the decoupling capacitor **Cc4** and is determined by the formula:

$$BW = \frac{g_m}{2\pi Cc}.$$

[0083] The high pass bandwidth **BW** must be maintained, as described above, at a level that is much, much smaller than the cutoff frequency of the cross-coupled differential oscillator to prevent loss of the fundamental frequency signal f_0. The decoupling capacitor **Cc** should be chosen such that the fundamental frequency f_0 of the cross-coupled differential oscillator is from approximately ten times to approximately twenty times the high pass bandwidth **BW** of the cross-

coupled oscillator.

[0084] Fig. 8 illustrates a quadrature oscillator having low phase noise of this invention. The cross-coupled differential oscillators **OSC1** and **OSC2** are structured and function as cross-coupled differential oscillators as described in Fig. 5a. The NMOS transistors **M3** and **M4** and the current sources **I3** and **I4** form a first coupling circuit. The current source **I3** is connected between the source of the NMOS transistor **M3** and the ground reference point. The current source **I4** is connected between the source of the NMOS transistor **M4** and the ground reference point. The gate of the NMOS transistor **M3** functions as the in-phase input of the first coupling circuit and the gate of the NMOS transistor **M4** functions as the out-of-phase input of the first coupling circuit. The drain of the NMOS transistor **M4** functions as the in-phase output of the first coupling circuit and the drain of the NMOS transistor **M3** functions as the out-of-phase output of the first coupling circuit. The decoupling capacitor **Cc6** is connected between the sources of the NMOS transistors **M3** and **M4**. The decoupling capacitor **Cc6** is chosen to function similar to the decoupling capacitor **Cc** of Fig. 5a to eliminate the phase noise from the first coupling circuit.

[0085] The in-phase input of the first coupling circuit is connected to the drain of the NMOS transistor **M5** and the gate of the NMOS transistor **M6** of the second cross-coupled differential oscillator **OSC2**. The out-of-phase input of the first coupling circuit is connected to the drain of the NMOS transistor **M6** and the

gate of the NMOS transistor **M5** of the second cross-coupled differential oscillator **OSC2**. The in-phase output of the first coupling circuit is connected to the drain of the NMOS transistor **M2** and the gate of the NMOS transistor **M1** of the first cross-coupled differential oscillator **OSC1**. The out-of-phase output of the first coupling circuit is connected to the drain of the NMOS transistor **M1** and the gate of the NMOS transistor **M2** of the first cross-coupled differential oscillator **OSC1**.

[0086] The NMOS transistors **M7** and **M8** and the current sources **I7** and **I8** form the second coupling circuit. The current source **I7** is connected between the source of the NMOS transistor **M7** and the ground reference point. The current source **I8** is connected between the source of the NMOS transistor **M8** and the ground reference point. The gate of the NMOS transistor **M7** functions as the in-phase input of the second coupling circuit and the gate of the NMOS transistor **M4** functions as the out-of-phase input of the second coupling circuit. The drain of the NMOS transistor **M7** functions as the in-phase output of the second coupling circuit and the drain of the NMOS transistor **M8** functions as the out-of-phase output of the second coupling circuit. The decoupling capacitor **Cc8** is connected between the sources of the NMOS transistors **M7** and **M8**. The decoupling capacitor **Cc8** is chosen to function similar to the decoupling capacitor **Cc** of Fig. 5a to eliminate the phase noise from the first coupling circuit.

[0087] The in-phase input of the second coupling circuit is connected to the drain of the NMOS transistor **M1** and the gate of the NMOS transistor **M2** of the first cross-coupled differential oscillator **OSC1**. The out-of-phase input of the second coupling circuit is connected to the drain of the NMOS transistor **M2** and the gate of the NMOS transistor **M1** of the first cross-coupled differential oscillator **OSC1**. The in-phase output of the second coupling circuit is connected to the drain of the NMOS transistor **M6** and the gate of the NMOS transistor **M5** of the second cross-coupled differential oscillator **OSC2**. The out-of-phase output of the second coupling circuit is connected to the drain of the NMOS transistor **M5** and the gate of the NMOS transistor **M6** of the second cross-coupled differential oscillator **OSC2**.

[0088] The in-phase and the out-of-phase of the first coupling circuit are transposed relative to the similar in-phase and out-of-phase connections of the second coupling circuit. This transposition is to force the necessary phase shift to cause the cross-coupled differential oscillators **OSC1** and **OSC2** to oscillate in quadrature or 90° out of phase as described above in Razavi.

[0089] The structure of the oscillator of Fig. 8 is generalized to a structure as shown in Fig. 9. This circuit is used to create multiple phased oscillators, mixers, modulators, demodulators, and any circuit requiring the transforming of the an input signal with multiple frequencies. The frequency transforming circuit of Fig. 9 has multiple coupling elements **CE1**, **CE2**, ..., **CEn** that are serially connected

output to input. The frequency transforming circuit, further, has multiple cross-coupled differential oscillators **OSC1**, **OSC2**, ..., **OSCn**. The output of each of the multiple cross-coupled differential oscillators **OSC1**, **OSC2**, ..., **OSCn** is connected to an input of one of the coupling elements coupling elements **CE1**, **CE2**, ..., **CEn**.

[0090] The input signal is developed between the input terminals **IN+** and **IN-** and is transferred to the first coupling element **CE1**. The input signal is then combined with the oscillatory signal from the first cross-coupled differential oscillator **OSC1**. The signal at the output of the first coupling element **CE1** is transferred to the input the second coupling element **CE2** where it is combined with the second oscillatory signal from the second cross-coupled differential oscillator **OSC2**. The signal at the output of the second coupling element **CE2** is transferred to the following coupling elements **CEn** for combination with the oscillatory signals from the subsequent oscillators **OSCn**. The signal from the final coupling element **CEn** is transferred to subsequent circuitry. In the alternative, the output of the last coupling element **CEn** maybe connected to the input of the first coupling element **CE1** to feedback the output signal (or a portion of the output signal) to the input of the circuit.

[0091] The coupling elements coupling elements **CE1**, **CE2**, ..., **CEn**, in addition to combining the oscillatory signals from the multiple cross-coupled differential oscillators **OSC1**, **OSC2**, ..., **OSCn**, may provide phase shifting for a

multiple phased oscillator, or any appropriate filtering, integrating, differentiating function.

[0092] Further, the outputs of each of the coupling elements **CE1**, **CE2**, ..., **CEn** is connected to an input of a buffering amplifier **BUF1**, **BUF2**, ..., **BUFn**. Each of the a buffering amplifiers **BUF1**, **BUF2**, ..., **BUFn** capture the output of one of the coupling elements **CE1**, **CE2**, ..., **CEn** and amplifies and isolates the signal to form the output signals ϕ_1, ϕ_2, ..., ϕ_n that are transferred to external circuitry.

[0093] Each cross-coupled differential oscillators **OSC1**, **OSC2**, ..., **OSCn**, each coupling element **CE1**, **CE2**, ..., **CEn**, and each buffering amplifier **BUF1**, **BUF2**, ..., **BUFn** has a differential amplifier with low phase noise of this invention as shown in Fig. 10. The differential amplifier is formed by the NMOS transistors **M1** and **M2** and the current sources **I1** and **I2**.

[0094] The gates of the NMOS transistors **M1** and **M2** respectively form the in-phase input **IN+** and the out-of-phase input **IN-**. The drains of the NMOS transistors **M1** and **M2** respectively form the in-phase output **OUT+** and the out-of-phase output **OUT-**.

[0095] The current source **I1** is connected between the source of the NMOS transistor **M1** and the ground reference point. The current source **I2** is connected between the source of the NMOS transistor **M2** and the ground reference point.

[0096] The decoupling capacitor **Cc** is connected between the sources of the NMOS transistors **M1** and **M2** to provide the necessary gain attenuating to eliminate the phase noise. When the differential amplifier is operating at sufficiently high frequency, the impedance of the decoupling capacitor **Cc** is very low and the current sources **I1** and **I2** combine. The differential amplifier operates as a true differential amplifier having very high gain. However, if the frequency of operation is sufficiently low, the impedance of the decoupling capacitor **Cc** is very high and the gain of the differential amplifier is very low, thus attenuating the signals of the phase noise.

[0097] The high pass bandwidth **BW** of the differential amplifier of this invention is a function of the transconductance (g_m) of the NMOS transistors "looking" into the sources and is determined by the formula:

$$BW = \frac{g_m}{2\pi Cc}.$$

For the most successful operation of the differential amplifier the decoupling capacitor **Cc** should be chosen such that the fundamental frequency f0 of the cross-coupled differential oscillator is from approximately ten times to approximately twenty times the high pass bandwidth **BW** of the cross-coupled oscillator. This insures that the fundamental frequency f0 is not affected by the operation of the decoupling capacitor **Cc**.

[0098] Fig. 11 is plots **700** and **750** that illustrate the spectral density of the phase noise of the output signal versus the frequency offset from the fundamental frequency f_0 of cross-coupled differential oscillators of this invention **700** and the prior art. As can be seen, the spectral density of the phase noise of the cross-coupled differential NMOS transistor is lower than an equivalent design of the prior art.

[0099] Fig. 12a is an example of an ideal current source utilized by the present invention. In Fig. 12a the ideal current source is implemented as a MOS transistor which is biased so that the MOS transistor operates in the saturation region. Such a current source may generate a 1/f noise component, which can be significant in MOS devices. This problem is exacerbated at higher frequencies, in which the oscillator of the present invention is designed to operate. Additionally, as the device geometry becomes small the 1/f noise becomes more pronounced. Fig. 12c illustrates an equivalent representation showing a current source I and a noise component current source I_{noise}

[00100] A conventional solution to reduce or eliminate the 1/f noise is to utilize a resistor as the current source. However, it is difficult to set the appropriate amount of resistance for the oscillator to function properly. In accordance with an embodiment of the present invention a programmable resistance R is utilized as the current source, as shown in Fig. 13a. The programmable resistance can insure the appropriate amount of resistance to provide the current to the

oscillator. The programmable resistance may be implemented as a switched resistor array. One example of the resistor array is shown in Fig. 13b. The resistor array shown therein comprises resistors R1-Rn and associated switches S1-Sn. Of course as will be appreciated by one of ordinary skill in the art, other resistor configurations may be employed and are within the scope and spirit of the present invention.

[00101] An alternative embodiment of the current source in accordance with the present invention is to utilize an inductance L in series with a programmable resistance R, as shown in Fig. 14a. As with the previous embodiment there is no 1/f noise, since the inductance and resistance are passive components. This configuration behaves like a constant current source regardless of the input voltage, especially if the inductance is sufficiently high, at high frequencies the current is essentially constant (due to the inductance properties). In this embodiment the programmable resistance may be implemented as a switched resistor array. One example shown therein comprises resistors R1-Rn and associated switches S1-Sn. Of course as will be appreciated by one of ordinary skill in the art, other resistor configurations may be employed and are within the scope and spirit of the present invention. The inductance L inherently has some resistance. Accordingly, the inductance and programmable resistance may be alternatively be implement by a switched inductance array, wherein each inductance inherently has the appropriate amount of resistance.

[00102] It will be apparent to those skilled in the art that the NMOS transistors **M1** and **M2** of Fig. 5a can be replaced by PMOS transistors with appropriate changes to the power supply voltage source V_{cc} and the ground reference point. Further, it would be apparent that the NMOS transistors could be replaced by bipolar junction transistors or other field effect transistors constructed of materials such as Galium-Arsenide and still be in keeping with this invention.

[00103] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.